Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A frequency synthesizing and back-end processing circuit, comprising:

a frequency synthesizer, operated by a clock signal, said frequency synthesizer including

a first multiplexer;

a first memory unit, coupled to said first multiplexer, for storing a first reference frequency;

a second memory unit, coupled to said first multiplexer, for storing a second reference frequency;

a shift register, forstoring a target frequency and comparing the target frequency with a predetermined value;

a control unit, coupled to said shift register, said control unit based on a result of comparing said target frequency with said predetermined value selecting one of said first reference frequency and said second reference frequency passes said first multiplexer;

a digital-to-analog converter,for converting a first signal passing through said first multiplexer to a second signal; and

a second multiplexer, based on a control signal passing one of said first signal and said second signal to obtain a third signal; and

a back-end processing circuit, including
a mixer, coupled to said second multiplexer for receiving said third signal; and
a filter, coupled to said mixer.

[c2] 2.The circuit of claim 1, wherein said shift register is a linear feedback shift register.

[c3] 3.The circuit of claim 2, wherein said result of comparing said target frequency with said predetermined value determines one of said first reference frequency and said second reference frequency passes said first multiplexer, said target frequency then shifts one bit responsive to said clock signal for comparing with said predetermined value again until a frequency resolution cannot distinguish a difference between said target frequency and said predetermined value.

[c4] 4. The circuit of claim 2, wherein the number of stages of said linear feedback shift register determines said frequency resolution, said frequency resolution is a ratio of a difference between said first frequency and said second frequency to a base 2 multiple exponential, said multiple is a number of said stages of said linear feedback shift register.

[c5] 5.The circuit of claim 1, wherein when said control signal

selects said first signal to pass through said second multiplexer, said mixer mixes said third signal and a signal generated by a numerical controlled oscillator.

[c6] 6.The circuit of claim 1, wherein when said control signal selects said second signal to pass through said second multiplexer, said mixer mixes said third signal and a signal generated by a voltage controlled oscillator.

[c7] 7. The circuit of claim 1, wherein said filter is a low pass filter.

[c8] 8.The circuit of claim 1, wherein said filter is a band pass filter.

[c9] 9.The circuit of claim 1, wherein said filter is a high pass filter.

[c10] 10.A method for frequency synthesizing and back-end processing, comprising:
a frequency synthesizing method, including applying interpolation to synthesize a synthesized frequency satisfying a predetermined resolution; and
a back-end processing method, including a mixing method and a filtering method.

[c11] 11. The method of claim 10,wherein said frequency synthesizing method further includes synthesizing a digital

signal and converting said digital signal to an analog signal.

[c12] 12.The method of claim 10, wherein said mixing method includes mixing with a signal generated by a numerical controlled oscillator.

[c13] 13.The method of claim 10, wherein said mixing method includes mixing with a signal generated by a voltage controlled oscillator.

[c14] 14. The method of claim 10, wherein said filtering method includes a low pass filtering method.

[c15] 15.The method of claim 10, wherein said filtering method includes a band pass filtering method.

[c16] 16.The method of claim 10, wherein said filtering method includes a high pass filtering method.